CLAIMS

What is Claimed is:

1. A method of making a semiconductor package comprising:

providing a semiconductor carrier comprising at least a first flexible appendage connected to the body portion; each flexible appendage having a top face and a bottom face; and the body portion having the top face and a bottom face, a first semiconductor device and a second semiconductor device, each having a front face and a back face, the first semiconductor device and the second semiconductor device connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage;

forming a first fold in the first flexible appendage so that the back face of the first semiconductor device overlies the back face of the second semiconductor device.

2. A method of making a semiconductor package as set forth in Claim 1 further comprising a forming a second fold so in the first flexible appendage that a portion of the bottom face of the first flexible appendage underlying the first semiconductor device also overlies the top face of the body portion.

3. A method of making a semiconductor package as set forth in Claim 2 further comprising bonding a semiconductor device to the body portion prior to forming the second fold, and wherein the first semiconductor device overlies the semiconductor device bonded to the body portion.

4. A method of making a semiconductor package as set forth in Claim 1, wherein there is no semiconductor device bonded to the body portion.

5. A method of making a semiconductor package as set forth in Claim 1, wherein the first semiconductor device further comprises a first alignment key and the second semiconductor device further comprises a second alignment key, and further comprising mating the first alignment key with the second alignment key when the back face of the first semiconductor device overlies the back face of the second semiconductor device.

6. A method of making a semiconductor package as set forth in Claim 5 further comprising forming at least one of the first alignment key and the second alignment key by depositing a raised feature on the back face of an associated semiconductor device.

7. A method of making a semiconductor package as set forth in Claim 5 further comprising forming both of the first alignment key and the second alignment key by depositing an associated raised feature on the back face of one of the first semiconductor device and second semiconductor device .

8. A method of making a semiconductor package as set forth in Claim 5 wherein the first alignment key comprises a raised feature spaced a distance from a side edge of the first semiconductor device.

9. A method of making a semiconductor package as set forth in Claim 8 wherein the second alignment key comprises a raised feature spaced a distance from a distance from a side edge of the second semiconductor device and wherein the second distance is shorter than the first distance.

10. A method of making a semiconductor package as set forth in Claim 5 wherein the first alignment key comprises a raised feature positioned near a side edge of the first semiconductor device.

11. A method of making a semiconductor package as set forth in Claim 10 wherein the second alignment key comprises a raised feature spaced a distance from a side edge of the second semiconductor device.

12. A method of making a semiconductor package as set forth in Claim 1 further comprising bonding the first semiconductor device to the second semiconductor device with an adhesive.

13. A method of making a semiconductor package as set forth in Claim 5 further comprising depositing an electric insulation layer on each of the first and second semiconductor device and thereafter forming the first alignment key on one of the first and second semiconductor device and forming the second alignment key on the other of the first and second semiconductor device.

14. A method of making a semiconductor package as set forth in Claim 13 wherein the forming of each of the first and second alignment key comprises depositing a material comprising copper.

15. A method of making a semiconductor package as set forth in Claim 13 wherein at least one of the first and second alignment key comprises a bump having a ring shape.

16. A method of making a semiconductor package as set forth in Claim 15 wherein at least one of the first and second alignment key comprises a bump having an "L" shape.

17. A method of making a semiconductor package as set forth in Claim 1 wherein at least one of the first and second semiconductor device further comprises an electrically conductive bump connecting the semiconductor device to the first flexible appendage.

18. A method of making a semiconductor package as set forth in Claim 1 wherein there is no spacer between the back face of the first semiconductor device and the back face of the second semiconductor device.

19. A method of making a semiconductor package as set forth in Claim 1 further comprising an electrical connector extending from the body portion.

20. A method of making a semiconductor package as set forth in Claim 1 wherein the body portion is flexible.

21. A method of making a semiconductor package as set forth in Claim 1 wherein the body portion comprises at least one of a ceramic, a fiberglass based board, a plastic and a polyimide.

22. A method of making a semiconductor package as set forth in Claim 1 wherein the carrier comprises a flexible circuit.

23. A method of making a semiconductor package as set forth in Claim 1 wherein the carrier comprises a polyimide.

24. A method of making a semiconductor package as set forth in Claim 1 wherein the carrier comprises an anisotropic conductive film.

25. A method of making a semiconductor package as set forth in Claim 1 wherein at least one of the first and second semiconductor device comprises a micro-electromechanical device.

26. A method of making a semiconductor package as set forth in Claim 1 wherein the second flexible appendage extends from the opposite side of the body portion.

27. A method of making a semiconductor package as set forth in Claim 1 wherein the second flexible appendage extends from the same side of the body portion as the first flexible appendage.

28. A method of making a semiconductor package as set forth in Claim 27 wherein the first flexible appendage and the second flexible appendage define a slot therebetween.

29. A method of making a semiconductor package as set forth in Claim 1 wherein the package further comprises a second flexible appendage extending from the body portion and further comprising a third semiconductor device and a fourth semiconductor device each connected to the second flexible appendage, the third semiconductor device and the fourth semiconductor device each having a front face and a back face, and wherein the second flexible appendage includes a top face and a bottom face, and wherein the third semiconductor device and the second semiconductor device are connected to the second flexible appendage with the front face of each of the third and fourth semiconductor device facing the top face of the second flexible appendage,

forming a first fold in the second flexible appendage so that the back face of the third semiconductor device overlies the back face of the fourth semiconductor device.

30. A method of making a semiconductor package as set forth in Claim 29 further comprising forming a second fold in the second flexible appendage so that the bottom face of the second flexible appendage overlies a portion of the bottom face of the first flexible appendage and so that the first, second, third and fourth semiconductor devices are stacked in overlying and aligned positions.

31. A method of making a semiconductor package as set forth in Claim 30 wherein the package further comprises a third flexible appendage extending from the body portion and further comprising a fifth semiconductor device and a sixth semiconductor device each connected to the third flexible appendage, the fifth semiconductor device and the six semiconductor device each having a front face and a back face, and wherein the third flexible appendage includes a top face and a bottom face, and wherein the fifth semiconductor device and the sixth semiconductor device are connected to the third flexible appendage with the front face of each of the fifth and sixth semiconductor device facing the top face of the third flexible appendage,

forming a first fold in the third flexible appendage so that the back face of the fifth semiconductor device overlies the back face of the sixth semiconductor device.

32. A method of making a semiconductor package as set forth in Claim 31 further comprising forming a second fold in the third flexible appendage so that the bottom face of the third flexible appendage overlies a portion of the top face of the body.

33. A method of making a semiconductor package as set forth in Claim 32 wherein the package further comprises a fourth flexible appendage extending from the body portion and further comprising a seventh semiconductor device and a eighth semiconductor device each connected to the fourth flexible appendage, the seventh semiconductor device and the eighth semiconductor device each having a front face and a back face, and wherein the fourth flexible appendage includes a top face and a bottom face, and wherein the seventh semiconductor device and the eight semiconductor device are connected to the fourth flexible appendage with the front face of each of the seventh and eighth semiconductor device facing the top face of the fourth flexible appendage,

forming a first fold in the fourth flexible appendage so that the back face of the seven semiconductor device overlies the back face of the eighth semiconductor device.

34. A method of making a semiconductor package as set forth in Claim 33 further comprising forming a second fold in the fourth flexible appendage so that the bottom face of the fourth flexible appendage overlies a portion of the bottom face of the third flexible appendage and so that the fifth, sixth, seventh and eighth semiconductor devices are stacked in overlying and aligned positions.

35. A method as set forth in claim 34 further comprising forming a fold in the boding portion so that the first, second, third, fourth, fifth, sixth, seventh and eighth semiconductor devices are in overlying and aligned positions.

36. A method as set forth in claim 1 further comprising forming a fold in the body portion.

37. A semiconductor package comprising a semiconductor carrier comprising at least a first flexible appendage connected to the body portion; each flexible appendage having a top face and a bottom face; and the body portion having the top face and a bottom face;

a first semiconductor device and a second semiconductor device, each having a front face and a back face;

the first semiconductor device and the second semiconductor device being connected to the first flexible appendage with the front face of each semiconductor device facing the top face of the first flexible appendage and the first flexible appendage having a first fold therein so that the back face of the first semiconductor device overlies the back face of the second semiconductor device.

38. A semiconductor package as set forth in Claim 37 further comprising a second fold formed in the first flexible appendage so that a portion of the bottom face of the first flexible appendage underlying the first semiconductor device also overlies the top face of the body portion.

39. A semiconductor package as set forth in Claim 38 further comprising a semiconductor device bonded to the body portion and wherein the first semiconductor device overlies the semiconductor device bonded to the body portion.

40. A semiconductor package as set forth in Claim 38 wherein there is no semiconductor device bonded to the body portion.

41. A semiconductor package as set forth in Claim 38 wherein the first semiconductor device further comprises a first alignment key and the second semiconductor device further comprises a second alignment key mateable with the first alignment key.

42. A semiconductor package as set forth in Claim 41 wherein one of the first alignment key and the second alignment key comprises a raised feature.

43. A semiconductor package as set forth in Claim 41 wherein each of the first and second alignment key comprise a raised feature.

44. A semiconductor package as set forth in Claim 41 wherein the first alignment key comprises a raised feature spaced a distance from a side edge of the first semiconductor device.

45. A semiconductor package as set forth in Claim 44 wherein the second alignment key comprises a raised feature spaced a distance from a side edge of the second semiconductor device and wherein the second distance is shorter than the first distance.

46. A semiconductor package as set forth in Claim 41 wherein the first alignment key comprises a raised feature positioned near a side edge of the first semiconductor device.

47. A semiconductor package as set forth in Claim 46 wherein the second alignment key comprises a raised feature spaced a distance from a side edge of the second semiconductor device.

48. A semiconductor package as set forth in Claim 37 further comprising an adhesive bonding the first semiconductor device to the second semiconductor device.

49. A semiconductor package as set forth in Claim 42 wherein each of the first semiconductor and second semiconductor each further comprises an electric insulation layer.

50. A semiconductor package as set forth in Claim 49 wherein each of the first and second alignment key comprises a bump comprising copper.

51. A semiconductor package as set forth in Claim 49 wherein at least one of the first and second alignment key comprises a bump having a ring shape.

52. A semiconductor package as set forth in Claim 51 wherein at least one of the first and second alignment key comprises a bump having a "L" shape.

53. A semiconductor package as set forth in Claim 37 wherein at least one of the first and second semiconductor device further comprises an electrically conductive bump connecting the semiconductor device to the first flexible appendage.

54. A semiconductor package as set forth in Claim 37 wherein there is no spacer between the back face of the first semiconductor device and the back face of the second semiconductor device.

55. A semiconductor package as set forth in Claim 37 further comprising an electrical connector extending from the body portion.

56. A semiconductor package as set forth in Claim 37 wherein the body portion is flexible.

57. A semiconductor package as set forth in Claim 37 wherein the body portion comprises at least one of a ceramic, a fiberglass based board, a plastic and a polyimide.

58. A semiconductor package as set forth in Claim 37 wherein the carrier comprises a flexible circuit.

59. A semiconductor package as set forth in Claim 37 wherein the carrier comprises a polyimide.

60. A semiconductor package as set forth in Claim 37 wherein the carrier comprises an anisotropic conductive film.

61. A semiconductor package as set forth in Claim 37 wherein at least one of the first semiconductor and second semiconductor device comprises a micro electromechanical device.

62. A semiconductor package as set forth in Claim 37 further comprising the second flexible appendage extending from the opposite side of the body portion.

63. A semiconductor package as set forth in Claim 37 further comprising a second flexible appendage extending from the same side of the body portion as the first flexible appendage.

64. A semiconductor package as set forth in Claim 63 wherein the first flexible appendage and the second flexible appendage define a slot therebetween.

65. A semiconductor package as set forth in Claim 37 further comprising a second flexible appendage extending from the body portion and further comprising a third semiconductor device and a fourth semiconductor device, each connected to the second flexible appendage, the third semiconductor device and the fourth semiconductor device each having a front face and a back face, and wherein the second flexible appendage includes a top face and a bottom face, and wherein the third semiconductor device and the second semiconductor device are connected to the second flexible appendage with the front face of each semiconductor device facing the top face of the second flexible appendage and the second flexible appendage having a first fold therein so that the back face of the third semiconductor device overlies the back face of the fourth semiconductor device.

66. A semiconductor package as set forth in Claim 65 wherein the second flexible appendage includes a second fold therein so that the bottom face of the second flexible appendage overlies a portion of the bottom face of the first flexible appendage and so that the first, second, third and fourth semiconductor devices are stacked in overlying and aligned positions.